SystemC: A User's Perspective, What's Working and What Needs to be Improved

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SystemC Uses

- Modeling interconnect & non-processor components
  - Architecture models (“Architect’s View”)
  - Functional models (“Programmer’s View”)
- Above are mixed and integrated with processor models for:
  - Architecture exploration
  - Early software development
  - Early (post-Si) system validation readiness
  - Early RTL verification
    - Testbench* and test development (with ESL DUT)
    - Application of system-level stimulus
      - Co-simulation
      - Co-emulation

* Testbenches primarily developed in SystemVerilog

What's Working

- Leadership position in the ESL industry
- Sufficient performance and flexibility to meet a spectrum of system level modeling needs
- Built on C++ (leverages expertise, tools)
- Open source proof-of-concept simulator
- IEEE Standardization
  - IP
  - Tools (1st generation)
  - Training/Consulting
- Ongoing evolution to meet emerging needs

What Needs Improved

- Define standard abstraction levels
- Define TLM interoperability standards
  - Communications, configuration, instrumentation, debug
  - Model leverage between abstraction levels
- Alignment with SPIRIT standard
  - Seamless progression to RTL
- 2nd-generation tools
  - Bus model (protocol) generation
  - Higher level synthesis
    - Coarse power/area estimation o.k. to start (for architecture exploration)
  - SystemC-specific profiler